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(71) Applicant: **FUJITSU LIMITED**
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

(72) Inventor: **Aso, Yasuhiro**
2-20-14-403, Nakamura-Kita
Nerima-ku, Tokyo 176(US)
Inventor: **Takahashi, Atsuhisa**
5-3, Nijigaoka 1-chome, Asao-ku
Kawasaki-shi,Kanagawa 215(US)
Inventor: **Kakuma, Satoshi**
101 Azeria-Haitsu, 2-738, Kosugi-Jinya-cho
Nakahara-ku, Kawasaki-shi, Kanagawa
211(US)
Inventor: **Uchida, Yoshihiro**
W-10-117, Fujitsu Nakahara House 426,
Shiboguchi
Takatsu-ku, Kawasaki-shi, Kanagawa 213(US)

(74) Representative: **Lehn, Werner, Dipl.-Ing. et al**
Hoffmann, Eitle & Partner Patentanwälte
Arabellastrasse 4
W-8000 München 81(DE)

(54) An ATM cell broadcasting system.

(57) A feature of this invention resides in an ATM (asynchronous transfer mode) cell broadcasting system used in ATM switches comprising switch matrices for exchanging ATM cells inputted from a plurality of input highways and outputting them to a plurality of output highways.

The ATM cell broadcasting system comprises: either

tag information adders (2-1, ... 2-X), provided at respective input terminals of the switch matrices (1-A), for adding tag information according to respective identifiers assigned to the ATM cells; or

ATM-cell-switching identifier determinant memories (3-1, ... 3-y), provided for respective switch elements in the switch matrixes (1-B), for storing determinant data enabling the switch elements to determine, from the identifiers of the ATM cells, which ones of the ATM cells to switch and output to their output highways.

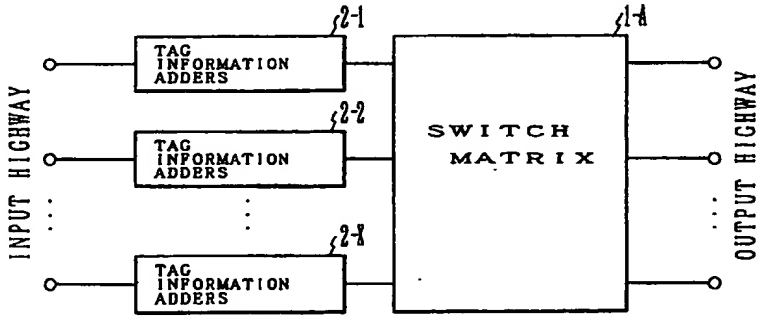

Fig. 1A

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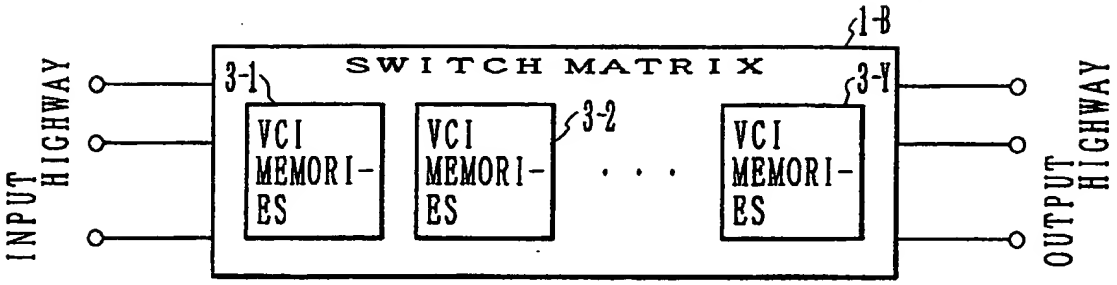
1-B
SWITCH MATRIX
3-1
3-2
3-Y
VCI MEMORIES
VCI MEMORIES
VCI MEMORIES
INPUT HIGHWAY
OUTPUT HIGHWAY

Fig. 1B

This invention pertains to a digital switching system, and more particularly to an ATM (Asynchronous Transfer Mode) cell broadcasting system utilized in ATM switches, e.g. for ISDN (Integrated Service Digital Network), which exchange ATM cells representing information having different traffic characteristics such as voices, data and moving images.

Description of the Related Art

With the recent widespread use of data communication, publicly switched networks now carry important data, as well as traditional voices, and are required to offer high-quality data transmission and exchange.

As a communication network for serving not only low speed data such as voice data, but also high speed data such as moving images, a broadband ISDN (B-ISDN) has begun to be put into practical use and various interfaces are being standardized. Unlike traditional switching methods, a B-ISDN utilizing an asynchronous transfer mode (ATM) can commonly carry various sorts of information at different speeds, e.g. voice data, moving image data and even continuous information mixed with burst information.

An ATM communication network transmits and exchanges information of different bands divided and housed in fixed-length data units called cells, instead of information divided and housed in variable-length packets used in traditional packet communication. Cells containing channel data are indiscriminately multiplexed, transmitted over optical fibers at high speed, and fast-exchanged by hardware switches. Thus, an ATM communication network can offer flexible services requiring different transmission speeds and makes efficient use of transmission paths.

User information is divided into several pieces according to its length and cells are configured by adding headers, e.g. of a few bytes, to the respective data, e.g. of 32 to 120 bytes, comprising the divided pieces of information. A header contains a virtual channel identifier (VCI) for identifying the originating user of the corresponding data. Thus, user information stored in cells is multiplexed over ATM highways before it is transmitted and exchanged. Switch elements in a switch matrix route cells to their respectively connected output highways, when they are turned on.

That is, a conventional switch matrix enables one-to-one communication by outputting an ATM cell inputted from an input highway to only one of a plurality of output highways. Therefore, there is a problem that it lacks the capacity for one-to-many communication, i.e. from one originator to a plurality of destinees, by outputting an ATM cell inputted from an input highway to a plurality of output highways.

Summary of the Invention

An object of the present invention is to bordcast data stored in cells to a plurality of destinees by outputting the cells to a plurality of output highways in an ATM switch.

An ATM (Asynchronous Transfer Mode) cell broadcasting system is utilized in ATM switches, e.g. for ISDN (Integrated Service Digital Network), which exchange ATM cells representing information having different traffic characteristics such as voices, data and moving images.

It configures a switch matrix, for exchanging ATM cells inputted from an input highway by outputting them to a plurality of output highways, to be provided with tag information adders, for adding to the ATM cells tag information corresponding to the VCI of the ATM cells, at its respective input terminals connected to input highways.

Brief Description of the Drawings

Figures 1A and 1B are block diagrams respectively illustrating a first and a second principle of this invention;

Figure 2 shows an exemplary configuration of an ATM cell;

Figure 3 is a block diagram showing the broadcasting system according to the first principle of this invention;

Figure 4 shows exemplary contents stored in a tag information memory;

Figure 5 is a flowchart of a switching judgment embodying the first principle of this invention;

Figure 6 is a block diagram showing the broadcasting system according to the second principle of this invention;

Figure 7 shows exemplary contents stored in an ATM-cell-switching VCI/VPi determinant memory for memorizing the VCI/VPi of the ATM cells to be switched; and

Figure 8 is a flowchart of a switching judgment embodying the second principle of this invention.

Description of the Preferred Embodiment

The first and second principles of this invention are explained by referring to Figures 1A and 1B, where switch matrices 1A and 1B output, to a plurality of output highways, ATM cells inputted from input highways by exchanging them.

Figures 1A and 1B are block diagrams respectively illustrating a first and a second principle of this invention.

In Figure 1A, tag information adders 2-1 through 2-X are converters provided at respective

N input terminals connected to input highways in a preceding stage of switch elements of switch matrix 1-A. They add to the ATM cells tag information for simultaneously outputting the ATM cells to a plurality of output highways corresponding to the VCI/VPi (indicating the originator) of the ATM cells. When switch matrix 1-A comprises e.g. 4*4 switch elements [for four (4) input highways and four (4) output highways], four (4) switch elements receive the same ATM cells from an input highway. If the tag information adder 3-i (where i is an integer from 1 to 4) corresponding to the input highway adds tag information, e.g. 0101, to the ATM cells, the second and fourth switch elements, e.g. from the input highway, are turned on and output the ATM cells to the output highways connected to these switch elements.

In Figure 1B, ATM-cell-switching VCI determinant memories 3-1 through 3-Y for memorizing the VCI of ATM cells to be switched are provided at the M switch elements in switch matrix 1-B. Upon receiving ATM cells, the M switch elements judge whether or not they should be turned on and output the ATM cells from the corresponding input highways to the corresponding output highways, by referring to the corresponding ATM-cell-switching VCI/VPi determinant memories 3-1 through 3-y. By variably setting routing information utilizing VCI/VPis in ATM-cell-switching VCI/VPi determinant memories 3-1 through 3-Y e.g. by software, the switch elements, whose ATM-cell-switching VCI/VPi determinant memories 3-1 through 3-Y have the same VCI/VPis as the ATM cells inputted from an input highway, output the ATM cells simultaneously to a plurality of output highways.

Thus, this invention enables ATM cells copied in a switch matrix to be transmitted simultaneously to a plurality of destinees.

Figure 2 shows an exemplary configuration of an ATM cell.

In Figure 2, an ATM cell has a total length of fifty-four (54) bytes. Its two (2) head end bytes store tag information for enabling the ATM cell inputted from an input highway to be outputted simultaneously to a plurality of output highways, according to the first principle of this invention. Next, after appropriate bytes for a virtual path number and the virtual channel number corresponding to a VCI, a maintenance datum of one (1) byte and message data from an originator of the remaining bytes are stored. According to the second principle of this invention, no tag information is required. Thus, the two (2) head end bytes remain empty.

Figure 3 is a block diagram showing the broadcasting system according to the first principle of this invention.

The switch matrix shown in Figure 3 comprises 4*4 switch elements for simplicity. In reality, a plurality of such switch matrices configure a large scale ATM switch. CNVs 10 through 40 are converters for converting to tag information the VCIs of ATM cells transmitted over corresponding input highways and enabling the ATM cells to be outputted to a plurality of output highways. On receipt of ATM cells, CNVs 10 through 40 read the tag information from a memory, not shown in the drawing, by using the VCI/VPis of the ATM cells. The bit length of tag information is equal to the number of switch elements receiving the ATM cells from a same input highway. In this case, since four (4) switch elements are connected to the each input highway through a converter, the tag information has four (4) bits. As shown in Figure 2, the tag information is attached to the ATM cells, which are inputted to switch elements (SWs) 11-A through 44-A connected to CNVs 10 through 40.

Assume here that ATM cells are inputted via CNV 10 to SWs 11-A through 14-A, CNV 10 converts the VCI of the ATM cells to 4-bit tag information 0101, and respective bits of tag information from the highest digit represent the flags of SWs 11-A through 14-A to be turned on. Since SWs 12-A and 14-A are turned on, they output the ATM cells to the output highways connected to them. Since SW 11-A and 13-A are not turned on, they do not output the ATM cells to the the output highways connected to them. Thus, the ATM cells of the same VCI inputted to CNV 10 are switched to two (2) of the four (4) output highways, and the ATM cells are broadcast to the intended destinees.

Figure 4 shows exemplary contents stored in a tag information memory.

CNVs 10 through 40 shown in Figure 3 refer to contents of a tag information memory. This invention purports to determine whence inputted ATM cells are outputted from the virtual path numbers and/or virtual channel numbers of the ATM cells. The tag information shown in Figure 4 is set according to the virtual path numbers and the virtual channel numbers. Although the example shown in Figure 4 illustrates a case in which both the virtual path numbers and the virtual channel numbers are of four (4) bits, ordinarily they are longer, e.g. of eight (8) bits or sixteen (16) bits.

Figure 5 is a flowchart of a switching judgment embodying the first principle of this invention. More specifically, Figure 5 is a flowchart of the switching judgment by SW NM-A, where N and M are any integers from 1 to 4. Since SW NM-A is located at the N-th position from the top and M-th position from the left in a switch matrix, it is connected with the N-th converter CNV.N0 and its flag is represented by the M-th bit from the highest digit of the tag information.

In Figure 5, after the processes begin, it is judged first whether the M-th bit from the highest

digit in the tag information is 0 or 1 , and the processes end without or after switching inputted ATM cells when it is 0 or 1.

Figure 6 is a block diagram showing the broadcasting system according to the second principle of this invention.

The configuration shown in Figure 6 is different from that in Figure 3, a block diagram showing the broadcasting system per the first principle of this invention, in that the former includes ATM-cell-switching VCI/VPi determinant memories 3-11 through 3-44 which store data for determining which ATM cells of VCIs are to be switched at the corresponding switch elements (SWs) 11-B through 44-B, whereas the latter instead includes CNVs 10 through 40 for converting the VCI/VPi of ATM cells inputted from the same input highway.

Figure 7 shows exemplary contents stored in an ATM-cell-switching VCI determinant memory for memorizing the VCI /VPi of the ATM cells to be switched.

In Figure 7, ATM-cell-switching VCI /VPi determinant memories 3-11 through 3-44 store, for respective addresses having bit lengths equal to the bit length of VCIs, 1-bit data of either 1 or 0 indicating whether or not the inputted ATM cells are switched to be outputted to the output highways corresponding to SW 11-B through 44-B.

Figure 8 is a flowchart of a switching judgment embodying the second principle of this invention.

In Figure 8, after the processes begin, data for the addresses corresponding to the VCIs of inputted ATM cells are read first from ATM-cell-switching VCI determinant memories 3-11 through 3-44, as shown in Figure 7, and the processes end without or after switching inputted ATM cells when it is 0 or 1.

As described so far, this invention enables ATM cells inputted from an input highway to be outputted simultaneously to a plurality of output highways, thereby enabling ATM cells to be broadcast to a plurality of destinees, which enhances the effectiveness of any communication system utilizing ATM cells.

Claims

1. An asynchronous transfer mode cell broadcasting system used in assynchronous transfer mode switches comprising:

   switch matrices for exchanging asynchronous transfer mode cells inputted from a plurality of input highways and outputting said asynchronous transfer mode cells to a plurality of output highways;

   tag information adding means, provided at respective input terminals of said switch matrices, for adding tag information according to respective identifiers assigned to said ATM cells so that said asynchronous trasfer mode cells are switched to a plurality of output highways based on said tag information.

2. The asynchronous transfer mode cell broadcasting system as set forth in claim 1, wherein:

   said tag information is added to the head portion of said asynchronous transfer mode cells for sequentially storing, after said tag information, virtual path numbers, virtual channel numbers, maintenance information, and user data.

3. The asynchronous transfer mode cell broadcasting system as set forth in claim 1, wherein:

   the bit length of said tag information corresponds to the number of switch elements connected to the respective one of said input terminals, which are connected to said input highways and provided with said tag information adding means;

   respective bits in said bit length indicate whether or not said switch elements in correspondence switch said asynchronous transfer mode cells inputted from said input highways; and

   said switch elements indicated by said bits in correspondence output said ATM cells to their output highways.

4. The asynchronous transfer mode cell broadcasting system as set forth in claim 1, wherein:

   said identifiers assigned to said asynchronous transfer mode cells are the respective virtual path numbers and/or virtual channel numbers of said asynchronous transfer mode cells.

5. The asynchronous transfer mode cell broadcasting system as set forth in claim 4, wherein:

   converters composing said tag information adding means add said tag information according to said virtual path numbers and/or virtual channel numbers.

6. An asynchronous transfer mode cell broadcasting system used in asynchronous transfer mode switches comprising switch matrices for exchanging asynchronous transfer mode cells inputted from a plurality of input highways and outputting them to a plurality of output highways, said asynchronous transfer mode cell broadcasting system comprising:

   asynchronous transfer mode-cell-switching identifier determinant memorizing means, provided for respective switch elements in said switch matrices, for storing determinant data

enabling said switch elements to determine, from the identifiers of said asynchronous transfer mode cells, which ones of said asynchronous transfer mode cells to switch and output to their output highways.

7. The asynchronous transfer mode cell broadcasting system as set forth in claim 6, wherein:

said identifiers assigned to said asynchronous transfer mode cells are the respective virtual path numbers and/or virtual channel numbers of said asynchronous transfer mode.

8. The asynchronous transfer mode cell broadcasting system as set forth in claim 7, wherein:

said asynchronous transfer mode-cell-switching identifier determinant memorizing means stores, at the addresses corresponding to said virtual path numbers and/or virtual channel numbers, said determinant data.

9. The asynchronous transfer mode cell broadcasting system as set forth in claim 8, wherein:

respective switch elements in said switch matrices refer to said asynchronous transfer mode-cell-switching identifier determinant memorizing means for storing said determinant data at said addresses corresponding to said virtual path numbers and/or virtual channel numbers of said asynchronous transfer mode cells inputted from said input highways connected to said switch elements; and

said switch elements output said asynchronous transfer mode cells to their output highways, when said switch elements determine, from said identifiers and said determinant data, to switch said asynchronous transfer mode cells.

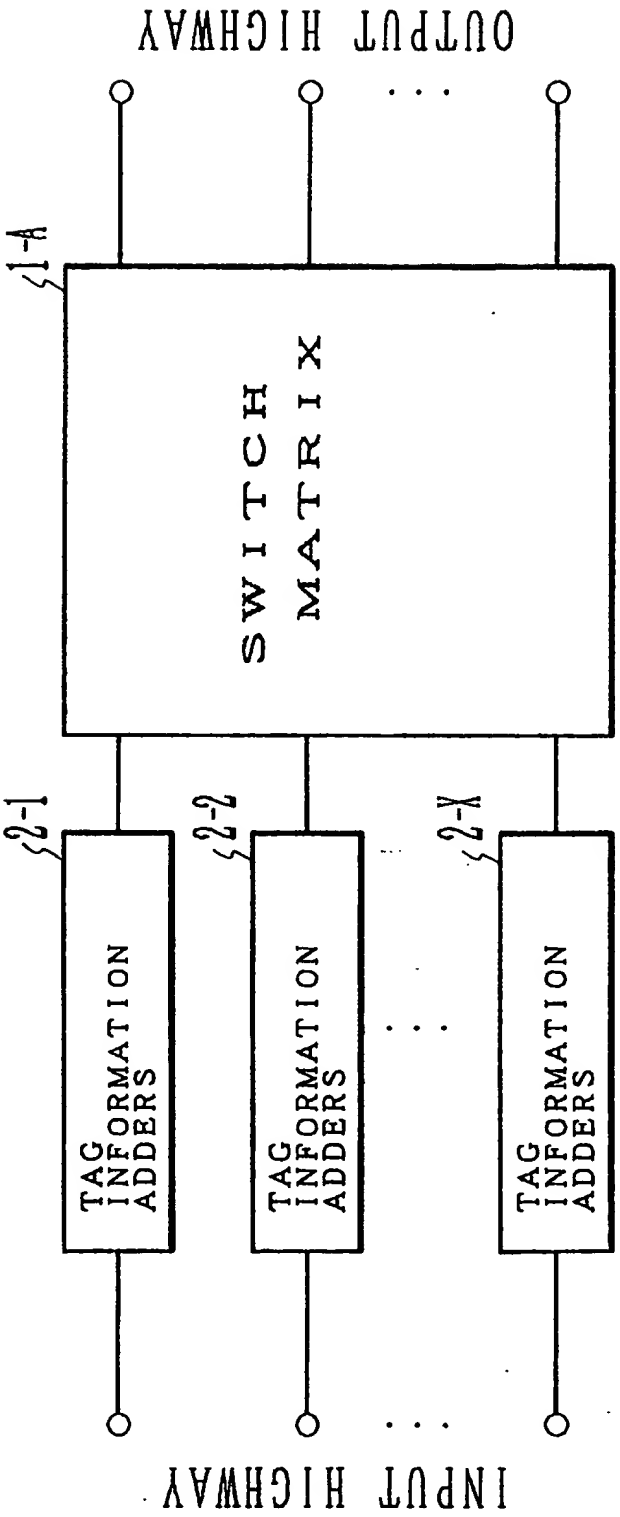
OUTPUT HIGHWAY
1-A
SWITCH MATRIX
2-1
2-2
2-X
TAG INFORMATION ADDERS
TAG INFORMATION ADDERS
TAG INFORMATION ADDERS
INPUT HIGHWAY

Fig. 1A

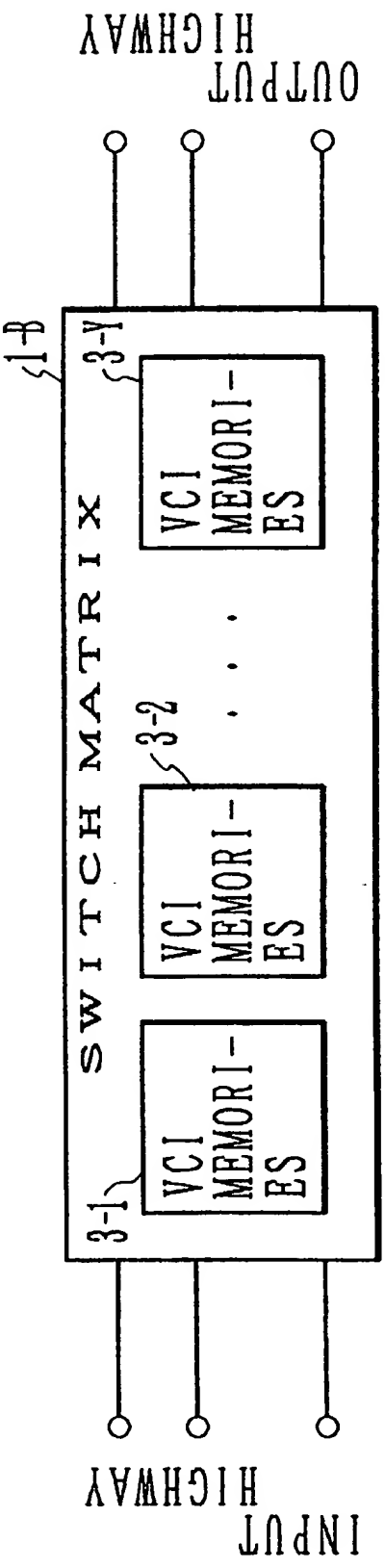
OUTPUT HIGHWAY
1-B
SWITCH MATRIX
3-Y
VCI MEMORIES
3-2
VCI MEMORIES
3-1
VCI MEMORIES
INPUT HIGHWAY

Fig. 1B

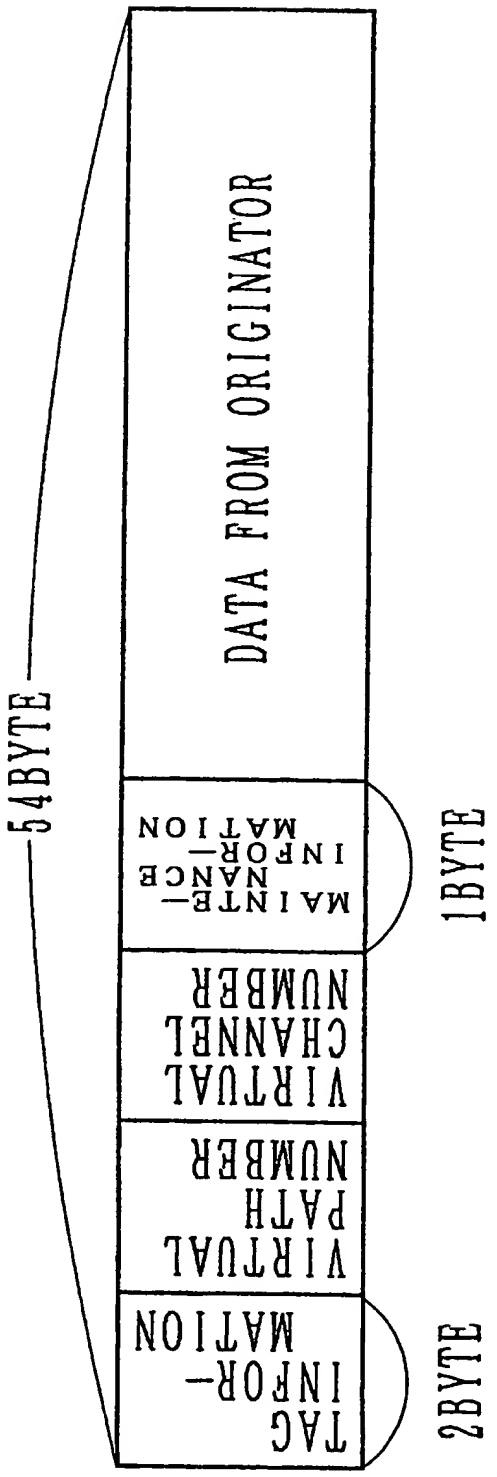
54BYTE
DATA FROM ORIGINATOR
MAINTE-
NANCE
INFOR-
MATION
1BYTE
VIRTUAL
CHANNEL
NUMBER
VIRTUAL
PATH
NUMBER
TAG
INFOR-
MATION
2BYTE

Fig. 2

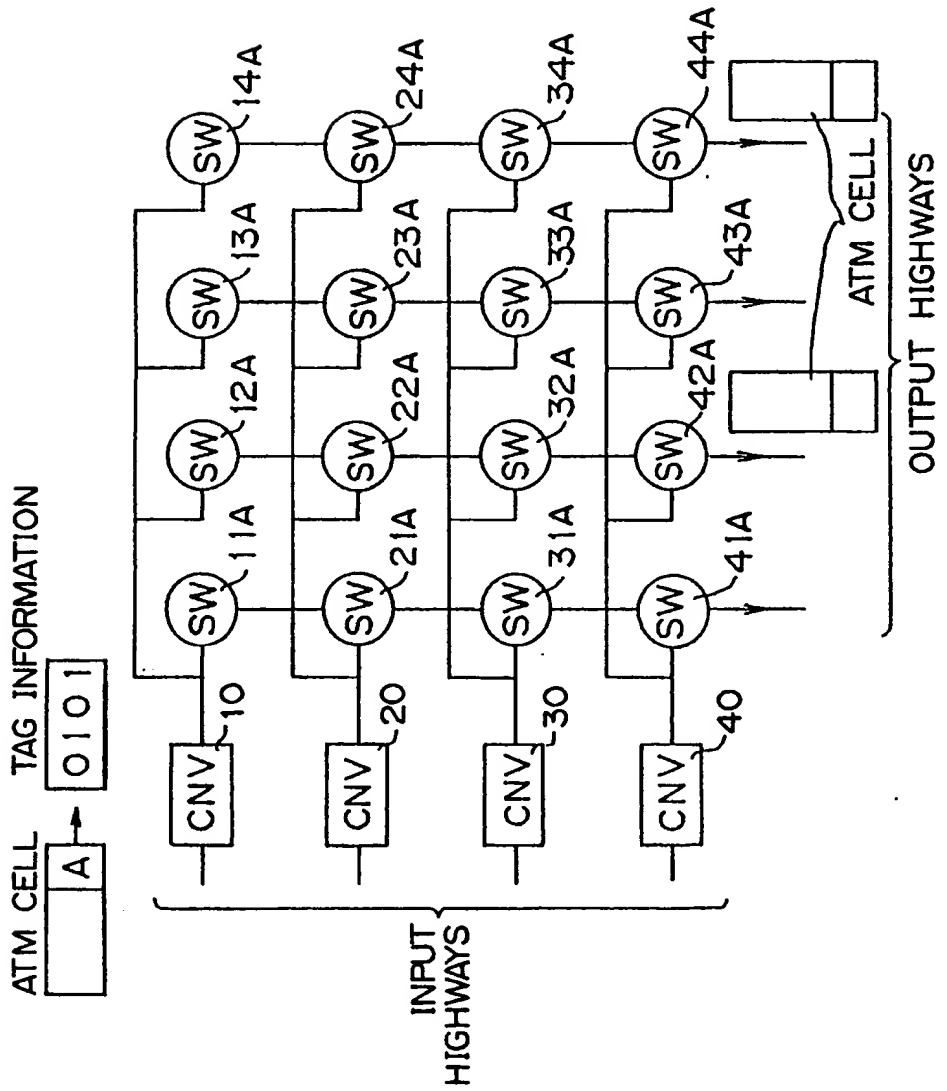
ATM CELL
A
TAG INFORMATION
0101
CNV
10
20
30
40
SW
11A
12A
13A
14A
21A
22A
23A
24A
31A
32A
33A
34A
41A
42A
43A
44A
INPUT HIGHWAYS
ATM CELL
OUTPUT HIGHWAYS

Fig. 3

VPI	VCI	TAG INFORMATION
0001	0001	0011
0001	0010	0101
•	•	•
•	•	•
•	•	•

Fig. 4

ADDRESS	DATA
000・・・・00	0
000・・・・01	1
•	
•	
•	
•	
111 10	
111・・・・11	0

Fig. 7

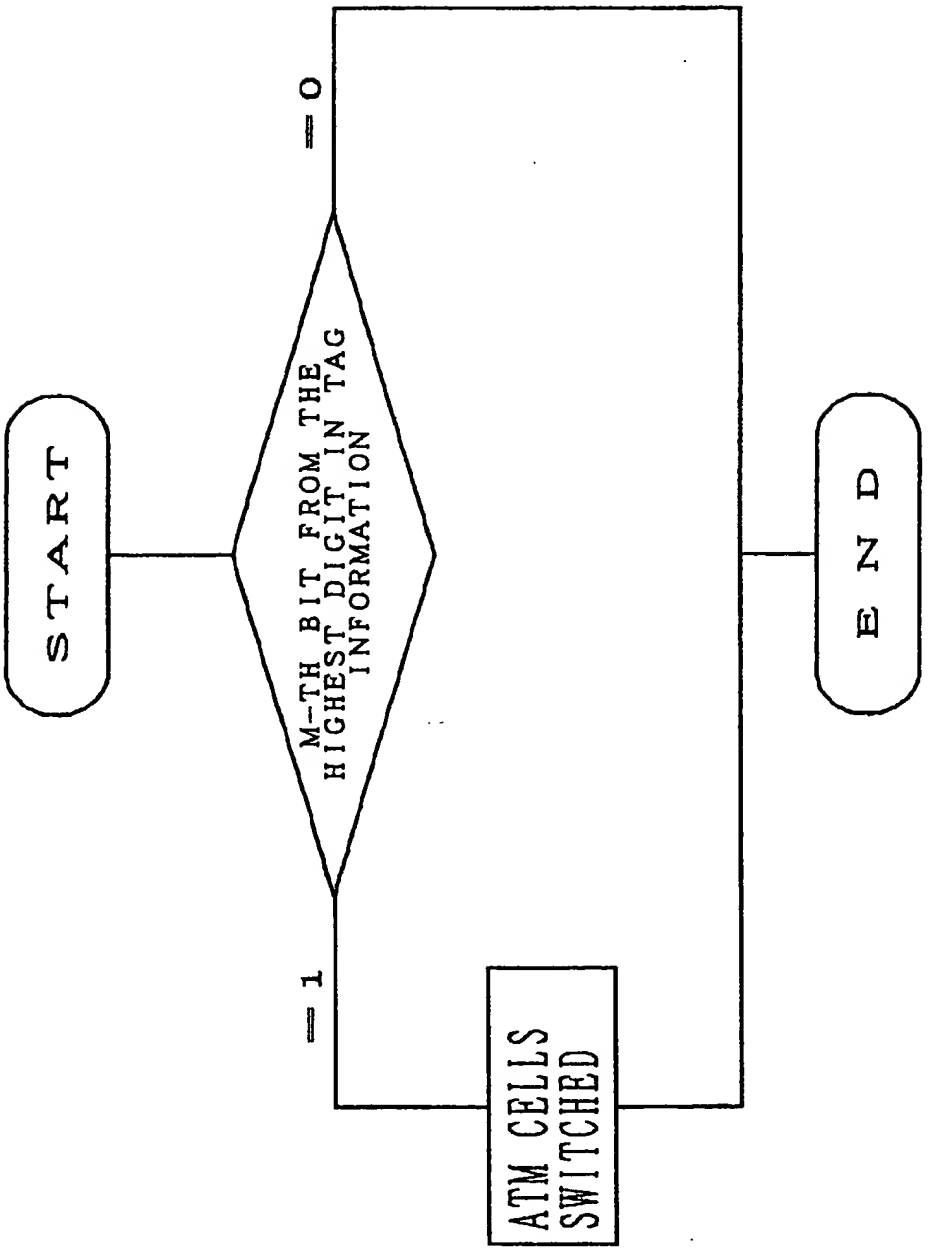
START
M-TH BIT FROM THE HIGHEST DIGIT IN TAG INFORMATION
= 0
= 1
ATM CELLS SWITCHED
END

Fig. 5

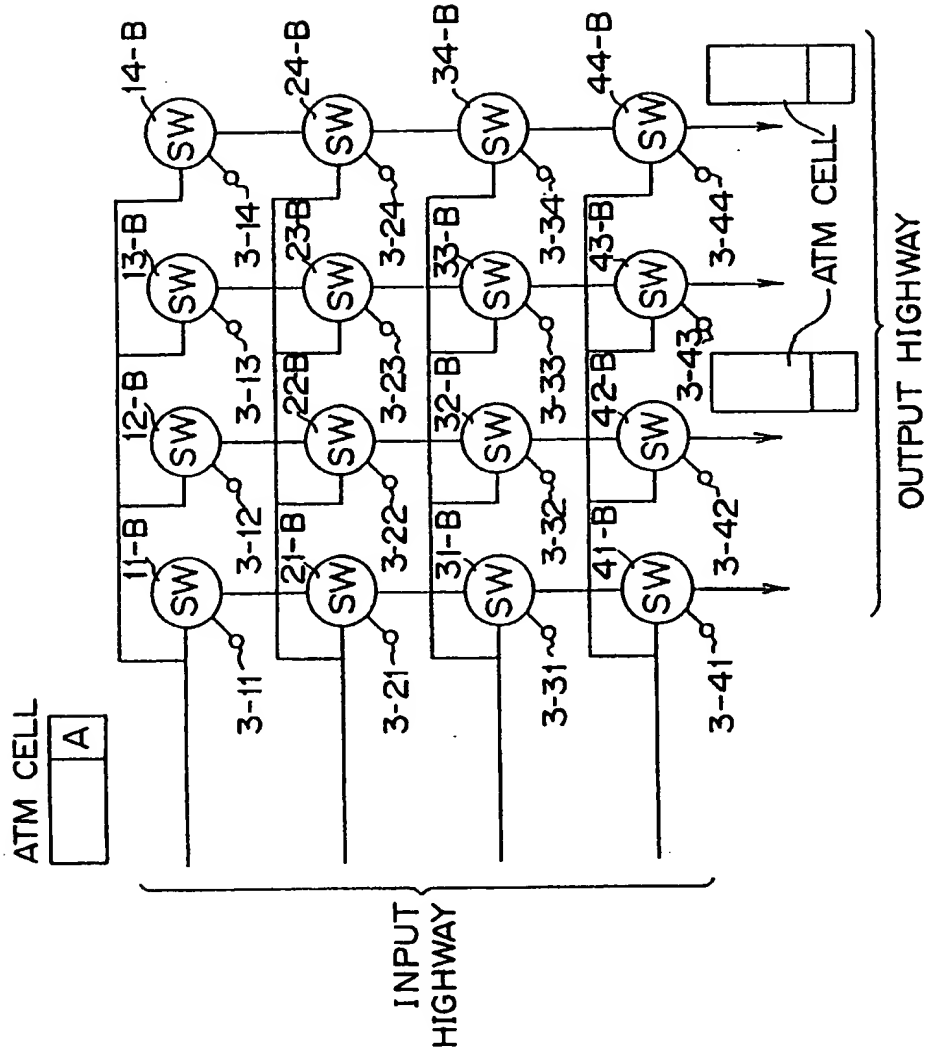
ATM CELL
A
INPUT HIGHWAY
OUTPUT HIGHWAY
ATM CELL
SW
11-B
12-B
13-B
14-B
21-B
22B
23B
24-B
31-B
32-B
33-B
34-B
41-B
42-B
43-B
44-B
3-11
3-12
3-13
3-14
3-21
3-22
3-23
3-24
3-31
3-32
3-33
3-34
3-41
3-42
3-43
3-44

Fig. 6

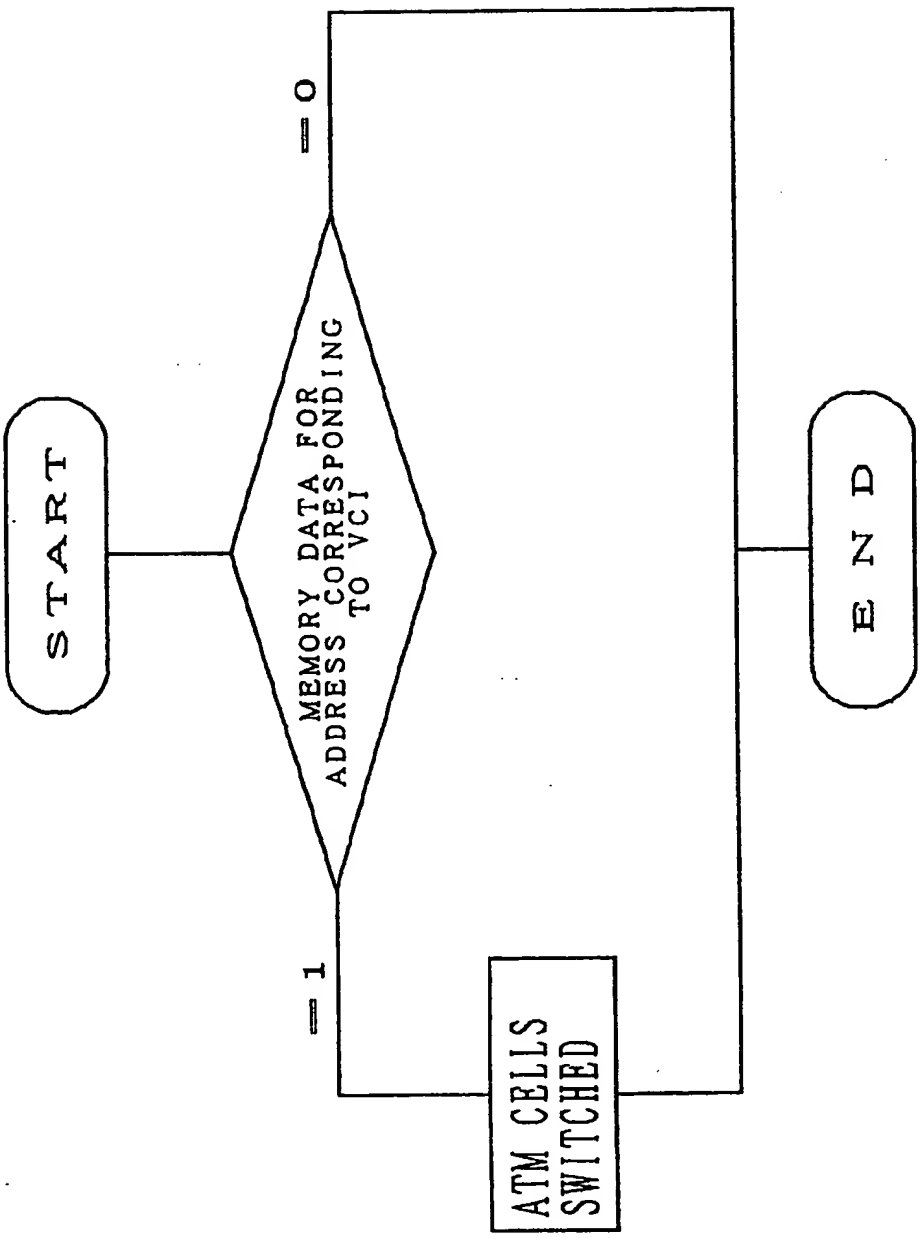
START
MEMORY DATA FOR ADDRESS CORRESPONDING TO VCI
= 0
= 1
ATM CELLS SWITCHED
E N D

Fig. 8